Sensing Schemes for STT-MRAMs structured with high TMR in low RA MTJs

Mesut Atasoyu, Mustafa Altun, and Serdar Ozoguz

Department of Electronics and Communication Engineering Istanbul Technical University, Istanbul,34469

Abstract

In this work, we investigated the sensing challenges of spin-transfer torque MRAMs structured with perpendicular magnetic tunnel junctions with a high tunneling magnetoresistance ratio in a low resistance-area product. To overcome the problems of reading this type of memory, we have proposed a voltage sensing amplifier topology and compared its performance to that of the current sensing amplifier in terms of power, speed, and bit error rate performance. We have verified that the proposed sensing scheme offers a substantial improvement in bit-error-rate performance. To enumerate the read operations of the proposed sensing scheme with the proposed cross-coupled capacitive feedback technique on the clamped circuity have successfully been performed a 2.5X reduction in average low power and a 13X increase in average reading speed compared with the previous works due to its device structure and the proposed circuit technique.

Keywords: PMA, MTJ, STT-MRAM, Sensing, BER, Low-power, High-speed

1. Introduction

Static random access memories (SRAM) are vital blocks of high-speed digital systems as these are used to implement on-chip cache memories. However, the static power consumption of SRAM increases while CMOS technology nodes are scaling down. The emerging non-volatile memories seem to be viable candidates to replace SRAMs in order to accommodate new scaled-down technologies. Among these memory candidates, spin-transfer torque magnetic RAM (STT-MRAM) is particularly attractive as it provides some unique advantages lacking in other candidates: CMOS compatibility, suitability for low-power and high-speed operations, and high endurance [1].

The storage device used in STT-MRAM is magnetic tunnel junction (MTJ) which allows the storage of the information via magnetoresistive effect, that is binary information is encoded in MTJ as high (R_{AP}) or low (R_P) resistance based on the relative magnetization directions of a ferromagnet. On the other hand, perpendicularly magnetized (PMA) MTJs offers the attractive feature of the low power switching property [1, 2, 3, 4, 5].

There are several types of PMA devices, which are the bulk PMA-MTJs in thin films, exchanged-coupled PMA-MTJs in superlattices, and interfacial PMA-MTJs (pMTJs) in ferromagnet(CoFe)/oxide(MgO) interfaces [6]. Among these, a pMTJ has attracted great attention for its potential benefits in realizing MTJ with high tunneling magnetoresistance(TMR) in low resistance area product (RA). Also, high TMR is better distinguishing the R_{AP} and the R_P states from each other, and low RA is better for reducing average switching current density [7]. In addition, TMR values depends on bias voltage [4] and temperature [3] variations. However, pMTJs with high TMR in low RA is challenging with high resistance variations due to their thinner tunnel barrier layer (MgO) [3, 4]. On the other hand, in write operations, the switching threshold current (I_C) of a pMTJ is an important parameter determining the current required to switch between the R_{AP} and R_P states. Low values of I_C are obtained while pMTJ dimensions are scaled down. However, scaling down the dimensions of pMTJ has its own drawbacks. These drawbacks often cause a read disturbance (RD) and incorrect decisions because of low sensing margin (SM) [1].

The purpose of this paper is to seek better sensing scheme solutions for recently proposed device methods [3, 4], whose devices have lower switching power than conventional devices. However, these MTJ devices have greater resistance variations such as 12.5% in this work than conventional MTJs, such as 5%, due to their thinner oxide thickness and their thinner free layer thickness. Our proposed sensing scheme has a balanced current mechanism that uses the cross-coupled capacitive feedback in the reference and data cells of the structured MRAM arrays. We verify the effectiveness of our technique by comparing exactly the same simulation framework with the seminal sensing scheme design [8], which is based on a current mode sensing scheme different from our design (voltage mode sensing scheme) and has reference cells of low cost MTJs whose resistance states are only in low resistance states, we have adopted this approach from [8]. The

☆Corresponding author Department of Electronics and Communication Engineering Istanbul Technical University, Istanbul,34469 .

☆☆Corresponding author. E-mail address: matasoyu@itu.edu.tr (M.Atasoyu) .

Monte Carlo BER results of the proposed sensing scheme and [8] show our contributions; Reducing MTJ dimensions requires reading operations of MRAM arrays at the low sensing current levels needed to prevent read disturbances due to the low switching current threshold value of MTJ between its high and low resistance states. Therefore, our sensing scheme enhances the BER performances comparing with [8] due to its well-defined the current values of data cells and reference cells. Secondly, we compare the voltage and the current mode sensing schemes in terms of power, speed and BER performances which are the main specifications for the sensing operations. This paper gives a perspective for ongoing sensing scheme designs for embedded MRAM in terms of a current mode and a voltage mode sensing scheme approaches.

In this work, we investigated the challenges of designing sensing schemes for STT-MRAM structured with high TMR pMTJs with low resistance area. To this end, we considered voltage and current sense amplifier topologies and evaluated their performances from different perspectives i.e. power dissipation, speed, and BER performances. However, the pMTJ in low resistance area features large resistance variations due to its thinner barrier oxide layer. This may substantially reduce the BER performance [3, 4] of the STT-MRAM arrays. As a remedy, we propose a circuit in which the sensitivity of the latch circuitry is improved, by retrieving the sense output from a high impedance node and by keeping the supply voltage headroom low which, in turn, enables low current sensing operation. Furthermore, we designed especially a clamped reference scheme in the proposed circuit in order to further improve BER performance. In the core design of the clamped reference circuitry, there is a cross-coupled capacitive feedback mechanism (CCCF) which reduces the hysteresis and kickback noise effects, as well as improves the current balancing between the data cells and the reference cells [8, 9, 10]. However, we have noticed that considering the effects of the parasitic capacitance compensation of the clamped reference circuitry increases the power consumption.

The rest of the paper is prepared as follows: Section 2 studies the compact modeling of the pMTJ, Section 3 shows the evolution of the proposed sensing scheme, Section 4 shows the simulation results and their effects on the key design metrics, Section 5 concludes this work.

2. The Compact Modeling of pMTJ

2.1. The physical Structure of pMTJ

An MTJ has three layers, which are a free layer (FL), a pinned layer (PL), and an oxide barrier layer (such as MgO). The device has two stable magnetic switchable resistance states which are a low resistance state (P) and a high resistance state (AP), stored in the FL. The magnetized state reversal of the MTJ can be either of a precessional nature or of the thermally activated switching nature. System speed mainly depends on the underlying switching mechanism, as is in precessional switching ($t_s \leq 3ns$), and in thermally activated switching ($t_s \geq 10ns$) [1]. The switching of these states depends on the magnetic polarization of the FL. If the magnetic polarization of FL is anti-parallel to PL, the state of MTJ is in an AP state; otherwise, it is parallel to the PL is a P state. If the current flows through the FL to the PL, the initial AP state switches to the P state via the STT effect. On the other hand, if the current flows from the PL to the FL, the initial P state switched to the AP state, as shown in Fig.1.

Table 1: MTJ Device Parameters

Parameter	**Value**
The spin polarization factor (P)	0.5
The memory cell area	40nmx40nm
The tunneling magneto resistance ratio (TMR)	165%
The oxide thickness (t_{ox})	1nm
The saturation magnetization (M_S)	800
Gilbert Damping(α)	0.007

2.2. The Simulation Framework

In this work, we use the macrospin compact model of MTJ written in Verilog-a [11], where the magnetic switching dynamics of the MTJ is described by LLGS equations in mono-domain [12] and the conductance of MTJ is modeled as described in [13]. In addition, 65nm CMOS model parameters and physical parameters of MTJs taken from [14, 15] are used in the models. The design parameters of the MTJ are given in Table-1. In addition, the configuration of the Monte Carlo Simulations with 1K samples is specified with the CMOS model of 65nm and the variation of t_{OX} of the MTJ is 2% (3σ). It is important to note that the resistance variations of MTJs are more than %12.

3. The Comparisons of Sensing Schemes for STT-MRAM

A sensing scheme of STT-MRAM adopts at its input a current or a voltage signal that enables to determine resistive information via a sense amplifier (SenseAmp), which can be a voltage-mode sense amplifier (VSenseAmp) or a current-mode sense amplifier (CSenseAmp). CSenseAmp amplifies the current difference between the activated bit line (BL) and the reference-line (REFL), while a VSenseAmp amplifies the voltage difference between the activated BL and the REFL. Comparing the speed of these SenseAmps, the reading time of a VSenseAmp takes

longer than a CSenseAmp due to a longer discharge or a longer charging time due to the large valued BL capacitance (C_{BL}) or the REFL capacitance (C_{REFL}). However, the reading operation of a VSenseAmp can be faster compared to CSenseAmp when the variations of threshold voltages V_{TH} of the CMOS devices are greater than 12mV [16]. In fact, the variations of V_{TH} are 30mV or more in deep sub-micron technologies [17], such as in 65nm CMOS technology nodes also used in this work [8, 18, 19, 17, 20]. It should be also noticed that these higher variations of V_{TH} substantially degrade sensing margin (SM).

In the literature, some works have been presented on improving the SM in order to reduce the BER. Some of these efforts are at the device level and rely on increasing the TMR of MTJs [21, 22, 6, 4, 3]. However, there are some efforts on circuit level based on equalizing the differences in parasitic resistance between BLs [8]. This latter approach improves the read access time [18] of well-defined reference resistance cells, which are self-reference cells [23], self reference cells with two transistors and two MTJs [17], dynamic data dependent reference cells [18, 24, 19], reference cells at only R_P state [8], and locating reference cells close to data cells [18]. At the same time, these works address the vulnerabilities of the sensing scheme of the STT-MRAM. However, the use of simple current mirror circuitry in the sensing scheme may increase current mismatches in the BLs and REFLs[8, 24, 19], and the dynamic data dependent sensing schemes [18, 24, 19] are a good solution to increase the SM, but the power consumption of these schemes increases due to the use of two cross-coupled latch SenseAmps [18, 24] and a differential amplifier [19]. In addition, these two latch circuits have a high sensitivity into the mismatches [19]. The realization of STT-MRAM cell arrays with two transistors and two MTJs [17] achieves low SM, whereas it suffers from high cost and high area. Although offset cancellation techniques can be used to improve SM further, all these techniques lead to power-hungry circuits[25], such proposed in [26].

4. The Proposed Sensing Schemes

The proposed VSenseAmp is composed of a latch, precharge and equalizing transistors, column (read enable) and write driver (write enable) switches, and clamped reference circuitry, as shown in Fig.1. The latch formed by cross-coupled inverter (M_{1-4}). Column equalizer transistors (M_{7-9}) sets BLs and REFLs to the same initial voltage value that is V_{DD}, especially, M_9 provides common feedback between BLs and REFLs. The write driver and the column selector switches form only NMOS transistors. The clamped reference circuitry formed by M_{C-R} transistors, and C_{1-2} capacitances, which are driven by VC (the value of 0,8V) and VR (the value of 0,7V) voltage sources.

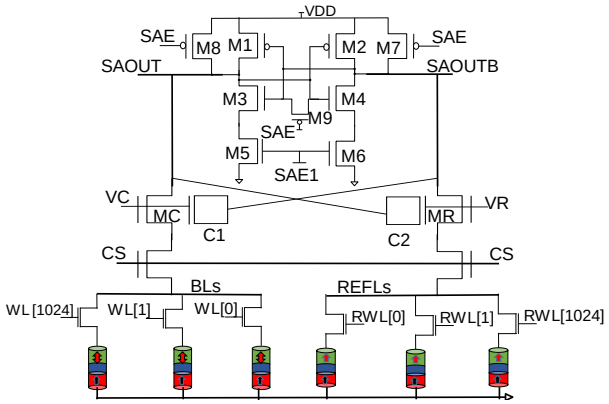

Figure 1: The schematic and array structure of the proposed SenseAmp.

4.1. The Power Efficient Timing of the proposed VSenseAmp

The reading operations of the proposed VSenseAmp are carried out in three phases: pre-charge, evaluation, and decision. The data and the reference cells are activated through word lines (WLs) and reference-WLs (REF-WLs). The activation orders for these stages are shown in Fig.2, the clock delays are similar to [8]. Also, the output signals of the proposed SenseAmp for the R_{AP} and R_P states are shown in Fig.2. In the pre-charge phase via M_{7-8}, transistors activated with the clock signal of SAE and further the latch is disconnected from the clock signal of SAE1 in order to reduce power dissipation [8]. Both BLs and RLs are pre-charged to the voltage value of $V_{DD} = 1V$, and also this voltage value can be possible in less than 1V in our proposed SenseAmp. In the evaluation and decision phases, the output of the proposed VSenseAmp goes to V_{DD}(goes to ground) when sensed resistive data from the activated STT-MRAM cell is high (low).

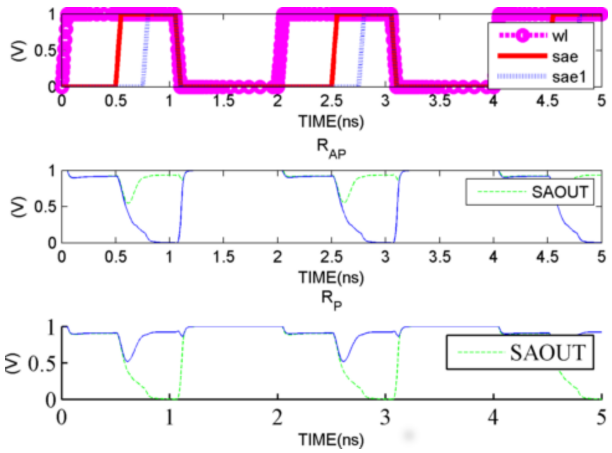

Figure 2: The timing diagrams of the proposed SenseAmp.

4.2. The CCCF: The Clamped Reference Neutralization Technique

The clamped reference circuitry was proposed more than two decades ago [9], but the researchers have a lot of attention due to its a cell current and a reference current protection mechanism, but especially at the low reading current levels in the emerging memory technologies (such as MRAM arrays), in our attempt, need to be modified it to obtain better determinations of the data cell and the reference cell currents by reducing the parasitic capacitances in the clamped reference circuitry that causes to wrong sensing results, according to our Monte Carlo BER simulation results. Furthermore, taking the outputs and inputs of the sense amplifier from the same nodes can help cancel out the effects of kickback noise and hysteresis noise [13]. More importantly, this design approach has a lower voltage headroom than the compared work [8] that is based on a current mode sensing scheme. Our work is a voltage mode sensing scheme that has better sensing results in the same simulation environment configuration taking into account a bit line and a reference line parasitic capacitances whose values are 50fF (given in section 5.3). We show that our design has immunity for the variation of sense amplifier output capacitances, which is namely memory effect.

The functions of the proposed clamped reference circuitry are as follows: to equalize the charging or discharging time of BLs and REFLs capacitances reducing the voltage swings on BLs and REFLs, balances the currents flowing on BLs and REFLs and cancels kickback noise [13], provides overcurrent protection [10, 8, 9], helps to a low resistance state sensing creating imbalance between BLs and REFLs because reference cells are only in low resistance state [8]. The circuit operations of these functions are as follows; MC and MR transistors are biased at the voltage values of $VC = 0.8$ and $VR = 0.7$ obtained via the parametric analysis for the optimal BER performance. These voltage sources drive the parasitic capacitances of MC and MR, mainly taking into account C_{GD}, and coupling of these capacitances to BLs and REFLs capacitances deteriorate the cell current, and so this can cause a read failure. Adding cross-coupled C_1 C_2 which are structured as a transistor that has the same width and length of transistors of MC or MR, as shown in Fig.1, helps to reduce these voltage fluctuations functioning as a capacitive voltage divider between BLs and REFLs, as formulated in Eq.1-2. However, this solution increases the occupied area of the sensing scheme.

$$\frac{V_{SAOUT} - VC}{V_{SAOUT} - V_{SAOUTB}} = \frac{C_{GDC}}{C_1 + C_{GDR}} \quad (1)$$

$$\frac{V_{SAOUTB} - VR}{V_{SAOUTB} - V_{SAOUT}} = \frac{C_{GDR}}{C_2 + C_{GDC}} \quad (2)$$

The resistance of the reference cell which is only a low resistance state in this work and [7] specifies a threshold voltage value between a high resistance state and a low resistance state of MRAM data cells that is a sensing margin. The threshold value will be zero when a data cell in low resistance state. These conditions can be circumvented with a clamped reference circuitry driven by different bias voltages. The sensing margin reduces with the resistance variations of the data and reference MRAM cells, CMOS device variations, parasitic capacitance, and resistance effects. In particular, the sensing margin has a small value with the reduced technology nodes of MTJ devices that because a high and a low resistance state has a closer resistance value. Therefore, the resistance of the clamped transistors which are driven by different bias voltages decreases the BER performance when sensing a low resistance state due to a parasitic capacitive coupling between gate to drain capacitors of the clamped transistors (MC and MR) to inputs of the sense amplifier. Therefore, in this paper, we propose to alleviate this penalty utilizing the current balance mechanism that is based on the cross-coupled feedback technique.

4.3. The Resistance Determination of Reference Cells

A current or a voltage signal difference between a data and a reference cell is amplified by SenseAmp; maximizing this signal difference improves the SM as well as a reference cell resistance with its low variation. Researchers have sought as a way to find well-defined reference cell resistance such as only R_P [8], current-mean [24, 9] and resistance-mean [24], dynamic data dependent [18, 24] and absolute resistance [27], and in this work, multiple-cell R_P building serially connected R_P to protect read-disturb.

5. Performance Comparisons

We compared the read performance of the CSenseAmp [8], our proposed VSenseAmp, and some SenseAmp designs in literature in terms of BER, power, speed, and area perspective. We perform the speed and power comparisons of our work with the reference works [18, 19, 23] taking into account the bit lines and the reference lines parasitic capacitance values of 50fF, and these simulation results are obtained from Monte Carlo analyses including CMOS device variations (TSMC 65nm physical parameters) and MTJ device variations. Moreover, intuitively speed and power performances of an MRAM cell can be better with MTJ or CMOS device level innovations, such used MTJ devices have lower switching power and a perpendicularly magnetized with low-resistance area product, proposed in [6, 3, 4]. We mentioned that this type of device has a better performance of speed and power.

5.1. The Read Realibility: BER Performances

The BER performances is given in this section to show the effectiveness of the proposed clamped reference neutralization technique on the voltage and the current mode sensing schemes in terms of their BER performance improvements. High TMR in low RA MTJ devices provides

resistance matching between MTJs and access transistors [21], as good as BER performance. However, TMR values are highly sensitive to variations of t_{OX} [3], free layer thickness (CoFe/CoFeB) [3], and RA product[4]. In addition, a pMTJ with a thinner t_{OX} has low RA product [3, 21], but has higher resistance variations. These resistance variations of pMTJs in our simulations are defined as 13% for both R_P (the actual value is 742Ω) and R_{AP} (the actual value is 1.97KΩ) according to t_{ox} thickness of 1nm with its variation of 2% for 3σ. It is important to note that the resistance variations of MTJ devices in simulations are generally defined as 5% and 3σ. In this work, they are so high because of the thinner thickness of t_{ox} as shown the mean variations of R_{AP} and R_P in Fig.6.

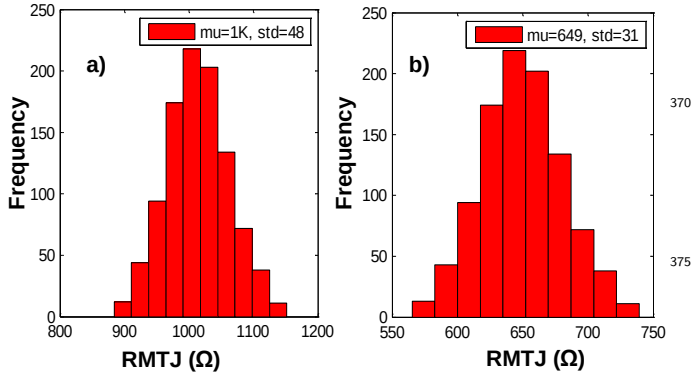

Figure 3: The resistance variations of the proposed pMTJ cells for a) The AP state b) The P state.

To improve BER performance, placing closer data and reference cells minimize resistance variations [18], but may consume extra area, and reducing secondary noise effects on the latch circuitry such as capacitive couplings, a kick-back, and a hysteresis noises [13]; on the other hand, the debate over the offset-aware design of a sensing scheme comes into conflict between a low power design or very precise design [25]. In this work, we compared the reference resistance scheme: serially stacked three pMTJs or one pMTJ in terms of their BER performance. In the serially stacked structure [28, 29], the reference resistance scheme combined serially connected three pMTJs, but has the same resistance value of one pMTJ, making the area of the one of this pMTJ is three times bigger than the area of one pMTJ. Indeed, this also provides unintentional write protection, due to three times increased J_C during reading operations. We compared the VSenseAmp and the CSenseAmp in terms of BER performance.

Furthermore, parasitic capacitance coupling effects on BER performance of the proposed VSenseAmp, such as hysteresis effects that causes the previous stored data on the C_{GD}) of the M3 and M4 causes when the recovery time of the latch is inefficient, concluded assuming the capacitances (taking such as 2fF, 4fF, 7fF) of the SAOUT and the SAOUTB nodes are initially set at the voltages of 0V (V_{DD}) then we sensed the stored R_{AP} (R_P) data. Also, these parasitic capacitance couplings of the proposed

Table 2: The comparison of different topologies based on the BER performances

Designs	R_P	R_{AP}
The CSenseAmp [8] with a single reference	427	0
The CSenseAmp with multiple references	17	6
The VSenseAmp with multiple references with CCCF	8	6
The VSenseAmp with a single reference with CCCF	2	8

VSenseAmp and the CSenseAmp [8] are shown in Fig.4.

The BER performance of the proposed VSenseAmp and CSenseAmp were evaluated by Monte Carlo simulations with CMOS 1K and MTJ using variation process samples. The proposed VSenseAmp is robust in secondary noise effects compared to the CSenseAmp, as shown in Fig.5 and Fig.6, which respond to AP and AP state detection. As a result, it is difficult to find an optimal solution in terms of the performance of REC between the states R_P and R_{AP} examining Table 2.

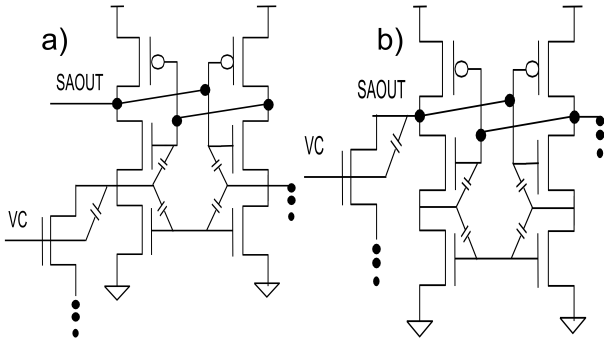

Figure 4: The parasitic capacitances: a) the CSenseAmp and b) the VSenseAmp.

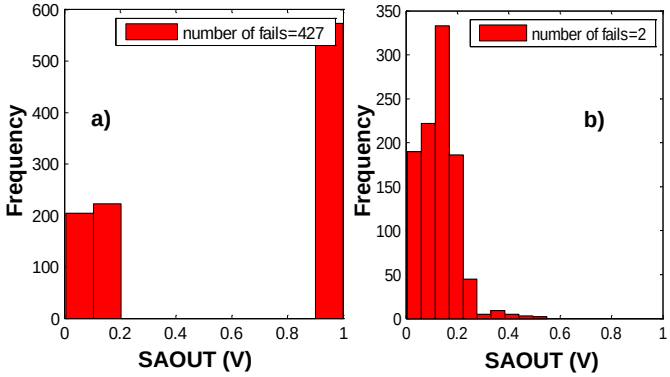

Figure 5: Monte Carlo Simulations for P states a) The CSenseAmp b) The proposed VSenseAmp.

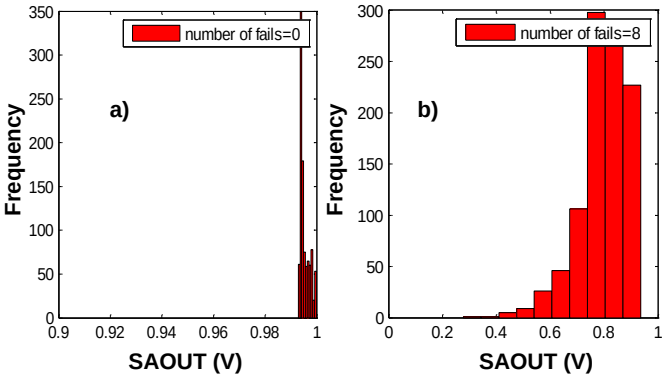

Figure 6: Monte Carlo Simulations for AP states a) The CSenseAmp b) Theproposed VSenseAmp.

Table 3: The comparison of the different topologies based on power(μW) consumptions

Designs	R_P (μW)	R_{AP} (μW)
The CSenseAmp [8] with a single reference	32	29
The VSenseAmp with a single reference	45	38
The VSenseAmp with multiple references	45	38
The VSenseAmp with CCCF with multiple references	48	41
The VSenseAmp with CCCF with a single reference	48	41

5.2. Power consumption comparisons

Firstly, the latch is a power-hungry unit and must be effectively disconnected via SAE1 clock after the sensing decision [8] for low power operation. We analyzed different timing strategies of SAE1 clock such as the same as the SAE clock or one or two inverter delays after SAE clock [10]; in fact, the most effective one is similar to [8], and also we applied our proposed VSenseAmp. However, the proposed CCCF technique increases the power consumption as given Table 3, and the CSenseAmp has less power consumption than the proposed VSenseAmp.In fact, reference resistance cells constructed with single MTJ and multiple MTJs have almost the same power dissipation, as indicated in Table 1. As a result, we compared the power dissipation (at 66.7MHz) of some previous works and the proposed VSenseAmp. Our proposed design has less power dissipation than these given works due to its device structure as well as the reduced capacitive coupling effects, as shown in Fig.4. In addition, our power dissipation results are obtained through Monte Carlo simulations (with 1K samples), and separately for the R_{AP} and R_P states.

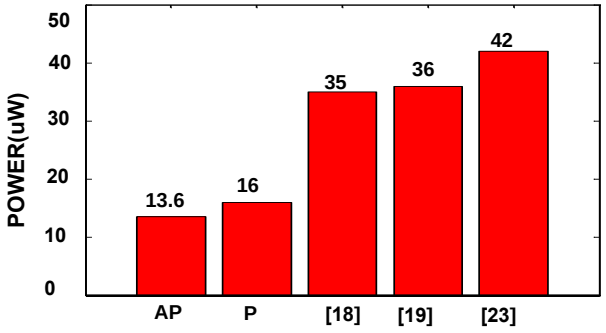

Figure 7: The power comparison of the previous works and the proposed VSenseAmp with CCCF.

5.3. Read speed comparisons

The speed comparisons are based on the simulations in HSPICE and are not included the parasitic word-line capacitances just only included the bitline parasitic capacitances as the value of 50fF that is higher than such a value of 30fF for 256 cells because the read access delay of the sensing scheme is a function of the bitline capacitances that is a $t_{access} = (C_{BL} * V_{offset})/I_{read}$ [30]. The readout time of the proposed VSenseAmp is sensitive to the discharging time of C_{BL} which was 50fF in our simulations, as well as to the voltage swings of BLs and REFLs. However, when a reading a word be needed to access the word-line with the write access delay specified to the process technology.

A VSenseAmp can be faster than a CSenseAmp when it is designed in deep submicron technology nodes [16]. The reading speed of a latched SenseAmp is limited by the overdrive recovery time of a latch circuitry that is needed for reliable sensing operations and also depends on the transconductance of M3 and M4 transistors and the parasitic capacitances. In order to improve the speed of the read operation of VSenseAmp, we have adopted a clamped reference scheme [10, 8], and we proposed the CCCF technique to improve the readout time. The proposed VSenseAmp is faster than the CSenseAmp and less sensitive to parasitic coupling capacitances, but read speed is not improved or deteriorated when a reference cell structured with single MTJ and multiple MTJs, according to our speed comparison results given in Table 4. In addition, these readout delay comparisons are not the same for the R_{AP} and R_P because of the asymmetric resistance distribution of R_{AP} and R_P. More importantly, the readout time of proposed VSenseAmp with CCCF is less sensitive to reference resistance variations taking account given speed comparison results in Table 4 for multiple and single reference schemes of the proposed VSenseAmp with or without CCCF; however, the proposed VSenseAmp with CCCF is slower but has a reliable operation. Indeed, the proposed VSenseAmp with CCCF has faster read operations than the compared CSenseAmp [8]. As a reminder, the high-speed operation will consume high power. As a result, our proposed VSenseAmp has better readout speed

Table 4: The comparison of different topologies based on the speed performances

Designs	$R_P(ps)$	$R_{AP}(ps)$
The CSenseAmp [8] with a single reference	656	707
The VSenseAmp without CCCF with a single reference	669	649
The VSenseAmp without CCCF with multiple references	167	151
The VSenseAmp with CCCF with multiple references	271	244
The VSenseAmp with CCCF with a single reference	270	244

performance among compared previous works, as shown in Fig.5, due to its device structure, less parasitic capacitance sensitivity and its current balance mechanism; as a note, our readout time values are mean values found in Monte Carlo simulation with 1K samples.

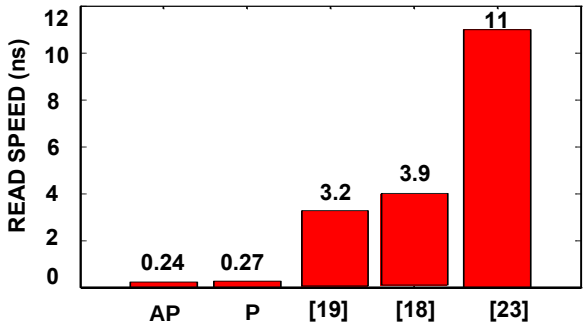

Figure 8: The readout delay times comparison of previous works with the proposed VSenseAmp with CCCF.

5.4. The outlook of chip area efficiency

The types of data and the reference cell arrays used in the implementation mainly determine the chip area of the STT-MRAM. The use of a common source-line array is an area-friendly approach compared to the approaches where the source-line is kept separated [18], or where the contact holes from BLs to access transistor are shared by the nearest cells [8]. The proposed VSenseAmp is thus an area-efficient design compared to circuits presented in [19, 18, 24]. The proposed VSenseAmp can be located at the edge of sub-array and can be shared between multiple BLs together. This approach may lead to further reduction in chip area [18]. As a reminder the layout of the proposed sensing scheme is not generated, this section is not concerned a layout-area comparison.

6. Conclusion And Discussions

In this work, we investigated the main limitations of sensing schemes designed for STT-MRAM structured with pMTJs providing high TMR in low resistance area. We have proposed a new sensing circuit, modified to address the main issues. It is important to notice that the proposed sensing scheme, i.e. the VSenseAmp is less sensitive to the resistance variations of the data and reference cells from the [8]. Moreover, the proposed VsenseAmp has a substantial advantage in sensing speed, BER compared to the counterparts of the proposed design in the literature and [8]. Consequently, the proposed VSenseAmp with a single reference pMTJ cell is a good solution for high-speed and low-power read operations. To enumerate the read operations of the proposed VSenseAmp with CCCF have successfully been performed a 2.5X reduction in average low power and a 13X increase in average high speed compared with the previous works due to its device structure and the proposed circuit technique. Our future work will examine specific circuit techniques to improve accuracy rates of the proposed VSenseAmp.

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